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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/825,973	04/05/2001	Norio Hirashita	OKI.227	3710

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EXAMINER	
MALDONADO, JULIO J	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 05/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/825,973	HIRASHITA ET AL.	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 23-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 23-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20040225*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The cancellation of claims 17-22 is acknowledged.

2. The addition of claims 31-34 is acknowledged.

3. Claims 1-16 and 23-34 are pending in the application.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3, 5, 7, 9, 11, 13, 15, 23-30 and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai (U.S. 6,344,675 B1).

Imai (Figs.12-13D) teach a low resistance SOI-FET device including an insulating layer (2); a semiconductor layer (3) formed on the insulating layer (2), wherein the semiconductor layer (3) includes the channel region therein; a pair of impurity layers (9, 10) formed in regions which are respectively in contact with the channel region in the source region and the drain region; and a pair of metallic silicide layers (16) respectively formed in the source region and the drain region, wherein the pair of metallic silicide layers (16) are respectively in contact with the pair of impurity layers (9, 10), wherein bottom surfaces of the pair of metallic silicide layers (16) extend to bottom surfaces of the semiconductor layer (3), wherein the thickness of the metallic silicide layers (16) is equal to or more than 80% of form an upper surface of the metallic silicide layers (16) to the bottom surface of the semiconductor layer; wherein the metallic silicide layers (16)

are composed of refractory metal and silicon, and wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, wherein the metallic silicide layer comprises cobalt silicide (column 22, line 66 – column 25 line 21 and column 43, line 6 – column 48, line 63).

Furthermore, Imai in another embodiment of the invention teaches wherein the source and drain regions extend between the cobalt silicide layers formed in said source and drain regions and the bottom surface of the semiconductor region (see, Fig.10).

Imai fails to expressly teach that the ratio of metallic silicide having the lowest resistance among stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following inequality: (X/Y) > (X0/Y0); wherein a ratio of cobalt to silicon is one to α ($1<\alpha<2$); and wherein a contact specific resistance between the metallic silicide layers and the impurity layers is less than $1x10^{-7}\Omega\text{-cm}^{-2}$. However, the selection of the claimed stoichiometric ratio and specific resistance is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species to obtain a desired conductivity. Therefore, it would have bee obvious to one of ordinary skill in the art at the time the invention was made to use the above-mentioned stoichiometric ratio and resistance to arrive at the claimed invention.

6. Claims 2, 4, 6, 8, 10, 12, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai ('675 B1) as applied to claims 1, 3, 5, 7, 9, 11, 13, 15 and 31-34 above, and further in view of the Applicants Admitted Prior Art.

Imai substantially teaches all aspects of the invention but fails to show wherein said FET device includes a depletion layer, which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof. However, the prior art teaches FET devices include a depletion layer, which expands to bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof (Instant pages 1 – 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Imai and the prior art to enable including the depletion layer of the prior art in the device of Imai.

Response to Arguments

7. Applicant's arguments filed 02/25/2004 have been fully considered but they are not persuasive.

Applicants' argue, "...the Imai reference provides no suggestion or motivation to modify the teaching therein to provide (1) that a ratio of metallic silicide having the lowest resistance among stoichiometric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the inequality: (X / Y) > (X0 / Y0); (2) a ratio of cobalt to silicon that is 1 to a ($1<\alpha<2$); or (3) a contact specific resistance between metallic silicide layers and impurity layers that is less than 1×10^{-7} - cm^2. The Examiner has merely alleged in hindsight that the selection of these claimed features would have been obvious by way of routine experimentation. However, there is no teaching, suggestion or motivation that can be found either explicitly or implicitly in the Imai reference, or any knowledge generally

available to one of ordinary skill established by the Examiner, that would lead one of ordinary skill to modify the Iwai teaching as suggested by the Examiner...".

In response to these arguments, as explained above, the selection of the claimed stoichiometric ratio and specific resistance is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species to obtain a desired conductivity. Specifically, Imai teaches forming low resistive region consisting of a metal silicide, wherein said metal silicide is selected from the group comprising cobalt silicide (Imai, column 23, lines 7 – 10 and column 43, lines 39 – 62). Furthermore, according to Yamanaka et al. (U.S. 5,915,187), the resistivity of a cobalt silicide layer depends on its ratio of cobalt to silicon (column 6, lines 15 – 24 and lines 55 – 61). Since one of the objectives in Imai is to form low resistive regions, the resistance of the cobalt silicide layer is a result-effective variable that depends on its ratio of cobalt to silicon and its determination of its optimum or workable ranges of said resistance might be characterized as routine experimentation. See MPEP 2144.05, IIA.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is 571-272-2800. See MPEP 203.08.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax number for this group is 703-872-9306 for before final submissions, 703-872-9306 for after final submissions and the customer service number for group 2800 is (703) 306-3329. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
May 6, 2004

George Fourson
Primary Examiner